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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/465,634	12/17/1999	DAVID K. VAVRO	INTL-0286-US	9115

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EXAMINER

MEONSKE, TONIA L

ART UNIT	PAPER NUMBER
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2181

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

09/465,634

Applicant(s)

VAVRO ET AL.

Examiner

Tonia L. Meonske

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 December 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4,6,7,9-16 and 18-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4,6,7,9-16 and 18-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless-
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 6, 9-16 and 18-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Balmer, US Patent 5,197,140 (herein referred to as Balmer), cited by Examiner on December 19, 2005.

3. Referring to claim 1, Balmer has taught a digital signal processor comprising:

a. a programmable, multiply and accumulate mathematical processor (Figure 4, elements 101-103, column 35, lines 39-56, columns 8-11, A multiply and an ALU operation is performed by each processor, elements 101-103, every cycle. An ALU operation is an accumulation.);

b. an input processor that processes input signals to the digital signal processor (Figures 2, 4, and 17, transfer processor and frame controllers, column 58, line 60- column 59, line 20, column 3, lines 10-17, column 11, line 55-column 12, line 12, column 4, line 60-column 5, line 13, column 7, lines 8-15. The input processor is the portion of the

transfer processor that processes a set of data input instructions from an external memory, see column 11, line 55-column 12, line 12.);

c. an output processor that processes output signals from the digital signal processor (Figures 2, 4, and 17, transfer processor and frame controllers, column 58, line 60- column 59, line 20, column 3, lines 10-17, column 11, line 55-column 12, line 12, column 4, line 60-column 5, line 13, column 7, lines 8-15, The output processor is the portion of the transfer processor that processes a set of data output instructions to an external memory, see column 11, line 55-column 12, line 12. Column 25, lines 20-34);

d. a master processor that controls said mathematical processor, said input processor and said output processor provides the timing for the other processors (Figures 2, 4, and 17, master processor, column 3, lines 10-17, column 4, line 60-column 5, line 5, column 12, lines 14-34);

e. a storage to store data from each of said processors so as to be selectively accessible by each of the processors (column 2, line 67-column 3, line 17, column 47- column 7, line 47); and

f. wherein each of said processors has a different instruction set than the other processors (The mathematical processor processes a set of low-level instructions, see column 14, line 47-column 15, line 18. The master processor processes a set of high-level instructions, including floating point operations, see column 14, line 47-column 15, line 18.

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The input processor is the portion of the transfer processor that processes a set of data input instructions from an external memory, see column 11, line 55-column 12, line 12. The output processor is the portion of the transfer processor that processes a set of data output instructions to an external memory, see column 11, line 55-column 12, line 12. Column 25, lines 20-34).

4. Referring to claim 2, Balmer has taught the digital signal processor of claim 1 further including a random access memory processor that stores intermediate calculation results (column 5, lines 47-61, see RAMS).

5. Referring to claim 3, Balmer has taught the digital signal processor of claim 2 including a bus coupling each of said processors to said storage (column 6, lines 39-52).

6. Referring to claim 4, Balmer has taught the digital signal processor of claim 1 wherein said input and output processors also implement mathematical operations (Figures 2,4, and 17, transfer processor and frame controllers, column 58, line 60-column 59, line 20 column 3, lines 10-17, column 11, line 55-column 12, line 12, column 4, line 60-column 5, line 13, column 7, lines 8-15).

7. Referring to claim 6, Balmer has taught the digital signal processor of claim 1 wherein said processors communicate with one another through said storage (column 2, line 67-column 3, line 17, column 47-column 7, line 47).

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8. Referring to claim 9, Balmer has taught the digital signal processor of claim 1 wherein said master processor waits for the input processor to complete a given operation (column 59, lines 12-20, column 11, line 55-column 12, line 12).

9. Referring to claim 10, Balmer has taught the digital signal processor of claim 1 wherein each of said processors includes its own random access memory (column 5, lines 47-61, see RAMS).

10. Referring to claim 11, Balmer has taught the digital signal processor of claim 1, as described above, and wherein said storage includes a plurality of registers, said registers automatically transfer existing data from a first register to a second register when new data is being written into said first register (column 43, line 50-column 45, line 52, saving the interrupt state).

11. Referring to claim 12, Balmer has taught the digital signal processor of claim 11, as described above, and wherein said input processor causes the automatic transfer of data (column 43, line 50-column 45, line 52, When an interrupt occurs, see "Packet Request", the state is saved.).

12. Referring to claim 13, Balmer has taught the digital signal processor of claim 11, as described above, and wherein said mathematical processor causes said data to be transferred from one register to another (column 43, line 50-column 45, line 52).

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13. Referring to claim 14, Balmer has taught the digital signal processor of claim 1 including a mathematical processor which is pipelined (column 39, lines 20-45).

14. Referring to claim 15, Balmer has taught the digital signal processor of claim 1 wherein said mathematical processor is a multi-cycled mathematical processor (column 39, lines 20-45, where an operation takes multiple cycles to complete. In this case a pipelined processor takes multiple cycles to complete.).

15. Claim 16 does not recite limitations above the claimed invention set forth in claim 1 and is therefore rejected for the same reasons set forth in the rejection of claim 1 above.

16. Claims 18-20 do not recite limitations above the claimed invention set forth in claims 11- 13 and are therefore rejected for the same reasons set forth in the rejection of claims 11 -13 above.

17. Referring to claim 21, Balmer has taught storing a bit which indicates which processor may control said automatic transfer of data from one register to another (column 50, lines 15-35; column 44, lines 34-67).

18. Claim 22 does not recite limitations above the claimed invention set forth in claim 14 and is therefore rejected for the same reasons set forth in the rejection of claim 14 above.

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19. Claims 23 and 24 do not recite limitations above the claimed invention set forth in claim 15 and are therefore rejected for the same reasons set forth in the rejection of claim 15 above.

Claim Rejections - 35 USC 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

21. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Balmer, US Patent 5,197,140 (herein referred to as Balmer), cited by Examiner on December 19, 2005.

22. Referring to claim 7, Balmer has taught the digital signal processor of claim 1, as described above. Balmer has not taught wherein each of said processors use very long instruction words. Employing this type of instruction format is well known in the art and would have allowed for several instructions of Balmer to be issued at once. Furthermore, by the nature of very long instruction words, the compiler would have only combined instructions that are not dependent upon one another. Issuing multiple independent instructions at once would have speed up the overall execution time of the processor by reducing the idle time of the processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention

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was made to employ the very long instruction word format for instructions issued to the plural processors of Balmer in order to increase speed and efficiency of those processors. Official notice has been taken.

Response to Arguments

23. Applicant's arguments filed December 13, 2006 have been fully considered but they are not persuasive.

24. On page 5, Applicant argues in essence:

"The material relied upon in the office action teaches away from the claimed invention. Specifically, the material relied on at column 14, line 47, is explicit that only two different types of processors are utilized. Thus, rather than teaching a different instruction set for each processor, the cited reference teaches making all of the processors one of two types, either the type for the master processor or the type for the other processors."

However, Examiner notes that at column 14, line 47, Balmer has not taught that only two different types of processors are utilized. Instead, Balmer has introduced the concept at line 47 that at least two different types of processors are necessary because of the level of processing, e.g. high level processing and low level processing. At least a high level processor and a low level processor are required. Furthermore, Balmer goes on to later state that the various low level processors take several different types of processors as required to perform the various instructions (see column 14, lines 64). So Balmer has not taught away from the claimed invention as argued by Applicant. Therefore this argument is moot.

25. On page 5, Applicant argues in essence:

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"The material cited with respect to the input processor (column 14, line 47 through column 15, line 18) does not in any way indicate that its instruction set is different from anything else."

However, the claimed input processor is interpreted to be the portion of the transfer processor of Balmer, element 11 of Figure 4, that processes input instructions. These input instructions comprise the claimed "instruction set" for the input processor. The input processor processes a set of instructions, or an "instruction set", to transfer data from an external memory to the internal memory (column 11, line 55-column 12, line 12). These input instructions, or the input processor's instruction set, are necessarily different than the master processor's instruction set that comprises a floating point arithmetic instruction set (see column 14, lines 49-64). Therefore the input processor's instruction set is at least necessarily different than the master processor's instruction set. Therefore this argument is moot.

Conclusion

26. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

27. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be

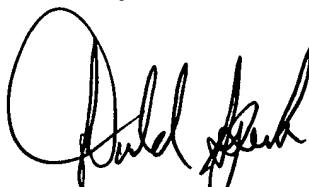
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calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday with first Friday's off.

29. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

30. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



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